Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

Claim 1 (Withdrawn): A method of manufacturing a semiconductor device according to claim 10, wherein

said step (b) forms first and second gate electrodes in respective partial areas of said first and second regions;

said step (c) implants impurities of the second conductivity type into a surface layer in said second region on both sides of said second gate electrode;

said step (d) forms first spacer films on side surfaces of said first and second gate electrodes; and

said step (e) implants impurities of said second conductivity type into surface layers in said first and second regions to form second impurity diffusion regions.

Claim 2 (Withdrawn): A method of manufacturing a semiconductor device according to claim 1, wherein said step (c) is executed after said step (f).

Claim 3 (Withdrawn): A method of manufacturing a semiconductor device according to claim 1, wherein each of said first to third activation processes includes a thermal treatment at a temperature at least equal to 750 °C.

Claim 4 (Withdrawn): A method of manufacturing a semiconductor device according to claim 1, further comprising steps of:

(h) forming second spacer films on the side surfaces of said first and second gate electrodes; and

(i) by using said second spacer films as a mask, forming a metal silicide layer on said first and second gate electrodes and on said second impurity diffusion regions.

Claim 5 (Withdrawn): A method of manufacturing a semiconductor device according to claim 1, wherein said third activation process is a laser thermal process.

Claim 6 (Withdrawn): A method of manufacturing a semiconductor device according to claim 5, wherein said process (g) comprises a step of forming an absorption layer which improves an absorption efficiency of laser radiated to said semiconductor substrate, a step of implanting impurity ions of the second conductivity type into at least said first region by using said first gate electrode as a mask, and a step of executing a thermal treatment by said laser thermal process.

Claim 7 (Withdrawn): A method of manufacturing a semiconductor device according to claim 1, wherein at least the first gate electrode is a dummy gate electrode, and the method further comprises, after said step (g), a step of forming an insulating film over said semiconductor substrate, said insulating film having etching characteristics different from material of said dummy gate electrode, and planarizing a surface of said insulating film to expose upper surfaces of said dummy gate electrode, a step of selectively removing said dummy gate electrode selectively with respect to said insulating film, and a step of burying conductive material in a space from which said dummy gate electrode has been removed.

Claim 8 (Withdrawn): A method of manufacturing a semiconductor device according to claim 1, wherein the gate length of said first gate electrode is shorter than the gate length of said second gate electrode.

Claim 9 (Withdrawn): A method of manufacturing a semiconductor device according to claim 1, wherein said first and second activation processes are executed at the same time.

Claim 10 (Currently Amended): A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having first and second regions of a first conductivity type defined by isolation regions in a principal surface area of the semiconductor substrate;

(b) forming at least a first gate electrode in a partial area of the first region;

(c) implanting impurities of a second conductivity type opposite to said first conductivity type into a surface layer of said second region, and thereafter executing a first activation process to form first impurity diffusion region shallower than said isolation regions;

(d) forming first spacer film on side surface of said first gate electrode;

(e) by using said first gate electrode and said first spacer film as a mask, implanting impurities of said second conductivity type into a surface layer of said first region, and thereafter executing a second activation process to form a second impurity diffusion region;

(f) removing said first spacer film; and

(g) by using said first gate electrode as a mask, implanting impurities of said second conductivity type into a surface layer in said first region, and thereafter executing a third activation process to form third impurity diffusion region, wherein said third activation process is executed so that the gradient of an impurity concentration distribution in a p-n junction formed by the third impurity diffusion region becomes steeper than the gradient of an impurity concentration distribution in a p-n junction formed by said first impurity diffusion region formed by said first activation process.

Claim 11 (Original) A method of manufacturing a semiconductor device according to claim 10, wherein each of said first to third activation processes includes a thermal treatment at a temperature at least equal to 750 °C.

Claim 12 (Original) A method of manufacturing a semiconductor device according to claim 10, wherein said third activation process is a laser thermal process.

Claim 13 (Previously Presented): A method of manufacturing a semiconductor device according to claim 10, said step (b) forms first and second gate electrodes in respective partial areas of said first and second active regions, and wherein the gate length of said first gate electrode is shorter than the gate length of said second gate electrode.

Claim 14 (Withdrawn): A method of manufacturing a semiconductor device according to claim 11, wherein said step (c) is performed after said steps (d) and (e).

Claim 15 (Withdrawn): A method of manufacturing a semiconductor device according to claim 14, wherein each of said first to third activation processes includes a thermal treatment at a temperature at least equal to 750 °C.

Claim 16 (Withdrawn): A method of manufacturing a semiconductor device according to claim 14, wherein said third activation process is a laser thermal process.

Claim 17 (Withdrawn – Previously Presented): A method of manufacturing a semiconductor device according to claim 14, said step (b) forms first and second gate electrodes in respective partial areas of said first and second active regions, and wherein the gate length of said first gate electrode is shorter than the gate length of said second gate electrode.

Claim 18 (Withdrawn): A semiconductor device comprising:

a semiconductor substrate having first and second regions of a first conductivity type defined in a principal surface area of the semiconductor substrate;

first and second gate electrodes formed in said first and second regions;

first SDE regions formed in surface layer on both sides of said second gate electrode and doped with impurities of a second conductivity type opposite to said first conductivity type;

second SDE regions formed in surface layer on both sides of said first gate electrode wherein the gradient of an impurity concentration distribution in a p-n junction formed by said second SDE regions is steeper than the gradient of an impurity concentration distribution in a p-n junction formed by said first SDE regions; and

source/drain regions formed on both sides of the first and second SDE regions wherein an impurity concentration distribution is the same in both p-n junctions formed by said source/drain regions in the first and second regions.

Claim 19 (Withdrawn): A semiconductor device according to claim 18, wherein a gate length of said first gate electrode is shorter than a gate length of said second gate electrodes.

Claim 20 (Withdrawn): A semiconductor device according to claim 18, further comprising a pocket implantation region of said first conductivity type at least in an area under each of said first SDE regions.

Claim 21 (Withdrawn): A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having a first region of a first conductivity type and a second region filled with an element separation insulating film, respectively defined in a principal surface area of the semiconductor substrate;

(b) forming a gate electrode at least in a partial area of the first region and a resistor layer made of material same as the gate electrode at least in a partial area of the second region;

(c) forming first and second spacer films on side walls of the gate electrode and the resistor layer;

(d) implanting impurities of a second conductivity type opposite to the first conductivity type into a surface layer in the first region by using the gate electrode and the first spacer films as a mask, and also into the resistor layer, and then executing a first activation process to thereby

form first impurity diffusion regions in the surface layer in the first region and lower a resistance of the resistor layer;

(e) removing the first and second spacer films; and

(f) implanting impurities of the second conductivity type into the surface layer in the first region by using the gate electrode as a mask, and then executing a second activation process to thereby form second impurity diffusion regions, wherein the second activation process is performed under a condition that a gradient of an impurity concentration distribution in a p-n junction in each of the second impurity diffusion regions becomes sharper than a gradient of an impurity concentration distribution in a p-n junction in each of the first impurity diffusion regions formed by the first activation process.

Claim 22 (Withdrawn): A method of manufacturing a semiconductor device according to claim 21, further comprising the steps of:

(g) forming a protective insulating film over the semiconductor substrate, the protective insulating film covering the gate electrode and the resistor layer;

(h) forming a mask covering the second region and thereafter anisotropically etching the protective insulating film to leave the protective insulating film on the side walls of the gate electrodes and in the second region;

(i) depositing a metal layer over the semiconductor substrate and executing a heat treatment to thereby form a metal silicide layer on an upper surface of the gate electrode; and

(j) selectively removing the unreacted metal layer on the protective insulating film.

Claim 23 (Withdrawn): A method of manufacturing a semiconductor device, comprising the steps of:

(a) preparing a semiconductor substrate having first and second regions of a first conductivity type and a third region filled with an element separation insulating film, respectively defined in a principal surface area of the semiconductor substrate;

(b) forming first and second gate electrodes at least in partial areas of the first and second regions and a resistor layer made of material same as the first and second gate electrodes at least in a partial area of the third region;

(c) implanting impurities of a second conductivity type opposite to the first conductivity type into the second region by using the second gate electrode as a mask and thereafter executing a first activation process to thereby form first impurity diffusion regions in a surface layer in the second region;

(d) forming first spacer films on side walls of the first and second gate electrodes and second spacer films on side walls of the resistor layer;

(e) implanting impurities of the second conductivity type at least in surface layers of the first and second regions by using the first and second gate electrodes and the first spacer films as a mask, and also into the resistor layer, and thereafter executing a second activation process to thereby form second impurity diffusion regions at least in the surface layer of the first or second region and lower a resistance of the resistor layer;

(f) removing the first and second spacer films; and

(g) implanting impurities of the second conductivity type into the surface layer in the first region by using the first gate electrode as a mask and thereafter executing a third activation process to thereby form third impurity diffusion regions, wherein the third activation process is

performed under a condition that a gradient of an impurity concentration distribution in a p-n junction in each of the third impurity diffusion regions becomes sharper than a gradient of an impurity concentration distribution in a p-n junction in each of the first impurity diffusion regions formed by the first activation process.

Claim 24 (Withdrawn): A method of manufacturing a semiconductor device according to claim 23, further comprising the steps of:

(h) forming a protective insulating film over the semiconductor substrate, the protective insulating film covering the first and second gate electrodes and the resistor layer;

(i) forming a mask covering the third region and partial areas in the first impurity diffusion regions and thereafter anisotropically etching the protective insulating film to leave the protective insulating film on the side walls of the first and second gate electrodes, in the second region, and in said partial areas;

(j) depositing a metal layer over the semiconductor substrate and executing a heat treatment to thereby form a metal silicide layer on an upper surface of the first impurity diffusion regions excepting said partial area and on upper surfaces of the first and second gate electrodes; and

(j) selectively removing the unreacted metal layer on the protective insulating film.

Claim 25 (Previously Presented): A method of manufacturing a semiconductor device according to claim 10, wherein said step (c) forms a resistor.

Claim 26 (Previously Presented): A method of manufacturing a semiconductor device according to claim 25, wherein said step (d) also forms a silicidation preventing film on the first impurity diffusion region.

Claim 27 (Previously Presented): A method of manufacturing a semiconductor device according to claim 12, wherein said first and second activating processes are done by rapid thermal annealing.

Claim 28 (Previously Presented): A method of manufacturing a semiconductor device according to claim 10, wherein the gradient of the impurity concentration distribution of the p-n junction formed by the third impurity diffusion region is steeper than the gradient of the impurity concentration distribution of the p-n junction formed by the second impurity diffusion region.